Seminar/Workshop
"Digital Embedded Systems in Research and Education"
Thursday 12th May and Wed 18th May 2016

Thursday 12th May
Room 230, SAPIENTIA - Hungarian University of Transylvania

Presentation Programme

09:00-09:05 dr. Laszlo BAKO, Sapientia,
Opening welcome

09:05-09:35 dr. Fearghal Morgan, National University of Ireland, Galway (NUI Galway)
"***viciLogic Online Learning, Assessment and GUI-based FPGA Prototyping Platform***"

09:35-10:00 dr. Piroska HALLER, Petru Maior Univ. Targu-Mures
"***Understanding computer architecture through prototyping***"

10:00-10:15 dr. Jozsef DOMOKOS, Sapientia
"***From Fundamentals of Digital Electronics to FPGA Based Digital System Design at the Department of Electrical Engineering of the Sapientia University***"

10:15-10:30 dr. Sandor-Tihamer BRASSAI, Sapientia
"***FPGA Embedded Systems Application in Robotics and Artificial Intelligence***"

10:30-10:50 dr. Laszlo BAKO, Sapientia
"***Applications of a versatile research tool and teaching platform: the FPGA circuit-based embedded system*** "

10:50-11:10 Coffee Break

Workshop I "Hands-on viciLogic online learning and viciLab for component-level FPGA prototyping and GUI-based real-time signal control and observation".
Presenter: dr. Fearghal Morgan (NUI Galway),
Collaborators: dr. Laszlo BAKO (Sapientia), drd. Szabolcs HAJDÚ, (Sapientia)
Lab 316, Sapientia

11:10-13:00 Hands-on introduction to the use of

- viciLogic online course browser, interacting with individual FPGA hardware engines, progressing through sample directed learning steps, and automatic knowledge check and assessment tasks
- viciLab for provided component-level remote and local FPGA prototype and GUI creation, controlling and observing all signals within the design in real time.
- viciLab for user-specific component-level or medium complexity FPGA prototype and GUI creation, controlling and observing all signals within the design in real time.
- Participants are invited to bring along
    - VHDL model for their own component or medium complexity design component
    - one or more block diagram(s) (png format, < 600*500 pixels). Block diagram(s) of design, illustrating top level and lower levels of design hierarchy. All internal signals will be presented to the user via the GUI in real time.

Wednesday, 18th May
Lab 316, SAPIENTIA - Hungarian University of Transylvania

Presentation/Workshop II "viciLogic/viciLab for Computer Architecture Education"
Presenter: dr. Fearghal Morgan (NUI Galway),
Collaborators: dr. Laszlo BAKO (Sapientia), drd. Szabolcs HAJDÚ, (Sapientia)

09:00-11:00

- Interactive presentation on viciLogic 16-bit processor learning and application development platform, and Integrated Development Environment (IDE) for program creation, assembly, execution, instruction-level debug, and visibility of all signals within the processor on each clock step.
- Develop a 16-bit processor program applications, and use the viciLab IDE and toolsuite to control and observe internal signal behaviour on each instruction.
- Overview of python-based GUI development for building viciLab applications